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Iyengar, A.;

Performance, Computing and Communications Conference, 1999. IPCCC '99. IEEE International , 10-12 Feb. 1999

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5 A new write-invalidate sn ping cache c herence prot c l f r split

transacti n bus-based multipr cess r systems*Seong Tae Jhang; Chu Shik Jhon;*

TENCON '93. Proceedings. Computer, Communication, Control and Power Engineering. 1993 IEEE Region 10 Conference on , Issue: 0 , 19-21 Oct. 1993
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Design and analysis of a scalable cache coherence scheme based on clocks and timestamps

Min, S.L. Baer, J.-L.

Dept. of Comput. Eng., Pusan Nat. Univ., South Korea;

This paper appears in: Parallel and Distributed Systems, IEEE Transactions on

Publication Date: Jan. 1992

On page(s): 25 - 44

Volume: 3 , Issue: 1

ISSN: 1045-9219

Reference Cited: 41

CODEN: ITDSEO

Inspec Accession Number: 4115872

Abstract:

A timestamp-based software-assisted cache coherence scheme that does not require any global communication to enforce the coherence of multiple private caches is proposed. It is intended for shared memory multiprocessors. The scheme is based on a compile-time marking of references and a hardware-based local incoherence detection scheme. The possible incoherence of a cache entry is detected and the associated entry is implicitly **invalidated** by comparing a clock (related to program flow) and a timestamp (related to the time of **update** in the cache). Results of a performance comparison, which is based on a trace-driven simulation using actual traces, between the proposed timestamp-based scheme and other software-assisted schemes indicate that the proposed scheme performs significantly better than previous software-assisted schemes, especially when the processors are carefully scheduled so as to maximize the reuse of cache **contents**. This scheme requires neither a shared resource nor global communication and is, therefore, scalable up to a large number of processors

Index Terms:

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Design and performance of a general-purpose software cache

lyengar, A.

IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA;

This paper appears in: Performance, Computing and Communications Conference, 1999. IPCCC '99. IEEE International

Meeting Date: 02/10/1999 - 02/12/1999

Publication Date: 10-12 Feb. 1999

Location: Scottsdale, AZ USA

On page(s): 329 - 336

Reference Cited: 9

Number of Pages: 498

Inspec Accession Number: 6196138

Abstract:

This paper describes a General-Purpose Software cache (GPS cache) which can improve the performance of many applications including Web servers and databases. It can service several hundred thousand cache hits per second on a uniprocessor. When used to cache data for a Web server accelerator, the overhead due to the GPS cache was an insignificant factor in the overall performance of the system. The GPS cache can store objects in memory, on disk, or both. The cache uses a new algorithm for managing expiration times of cached objects which is more efficient than previous ones. The GPS cache uses Data **Update** Propagation (DUP) to **invalidate** complex objects which is crucial for caching and maintaining **updated** copies of dynamic Web pages. Transactions can be logged using different buffering mechanisms in order to provide a balance between efficiency and currency of transaction log files. The GPS cache provides API functions which allow applications to directly manipulate its **contents**

Index Terms:

[cache storage](#) [performance evaluation](#) [search engines](#) [GPS cache](#) [General-Purpose Software cache](#) [Web server accelerator](#) [Web servers](#) [buffering mechanisms](#) [overhead](#) [performance](#) [software cache](#)

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Energy-efficient caching for wireless mobile computing

Kung-Lung Wu Yu, P.S. Ming-Syan Chen

IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA;

This paper appears in: Data Engineering, 1996. Proceedings of the Twelfth International Conference on

Meeting Date: 02/26/1996 - 03/01/1996

Publication Date: 26 Feb.-1 March 1996

Location: New Orleans, LA USA

On page(s): 336 - 343

Reference Cited: 11

Inspec Accession Number: 5242633

Abstract:

Caching can reduce the bandwidth requirement in a mobile computing environment. However, due to battery power limitations, a wireless mobile computer may often be forced to operate in a doze (or even totally disconnected) mode. As a result, the mobile computer may miss some cache **invalidation** reports broadcast by a server, forcing it to discard the entire cache **contents** after waking up. In this paper, we present an energy-efficient cache **invalidation** method, called GCORE (Grouping with COLD **update-set** REtention), that allows a mobile computer to operate in a disconnected mode to save the battery while still retaining most of the caching benefits after a reconnection. We present an efficient implementation of GCORE and conduct simulations to evaluate its caching effectiveness. The results show that GCORE can substantially improve mobile caching by reducing the communication bandwidth (or energy consumption) for query processing

Index Terms:

[cache storage](#) [client-server systems](#) [data integrity](#) [network servers](#) [power consumption](#) [query processing](#) [wireless LAN](#) [GCORE](#) [bandwidth requirement](#) [battery power limitations](#) [cache invalidation reports](#) [caching effectiveness evaluation](#) [cold update-set retention](#) [communication bandwidth reduction](#) [disconnected mode](#) [doze mode](#) [energy consumption](#) [energy-efficient caching](#) [grouping](#) [query processing](#) [reconnection](#) [simulations](#) [wireless mobile computing](#)

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Pages: 336 - 343

Year of Publication: 1996

ISBN:0-8186-7240-4

Authors

[Kun-Lung Wu](#)[Philip S. Yu](#)[Ming-Syan Chen](#)

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Bit-sequences: an adaptive cache invalidation method in mobile client/server environments

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 Pages: 115 - 127
 Year of Publication: 1997
 ISSN:1383-469X

Authors [Jin Jing](#) Mobile Communication Operations, Intel Corporation, 2511 NE 25th Avenue, Hillsboro, OR
[Ahmed Elmagarmid](#) Department of Computer Sciences, Purdue University, West Lafayette, IN
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↑ ABSTRACT

In this paper, we present Bit-Sequences (BS), an adaptive cache invalidation algorithm for client/server mobile environments. The algorithm uses adaptable mechanisms to adjust the size of the invalidation report to optimize the use of a limited communication bandwidth while retaining the effectiveness of cache invalidation. The proposed BS algorithm is especially suited for dissemination-based (or "server-push"-based) nomadic information service applications. The critical aspect of our algorithm is its self-adaptability and effectiveness, regardless of the connectivity behavior of the mobile clients. The performance of BS is analyzed through a simulation study that compares BS's effectiveness with that of a hypothetical optimal cache invalidation algorithm.

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Note: OCR errors may be found in this Reference List extracted from the full text article. ACM has opted to expose the complete List rather than only correct and linked references.

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2 [Swarup Acharya , Michael J. Franklin , Stanley B. Zdonik, Disseminating Updates on Broadcast](#)


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static ones, since applications can explicitly **invalidate** any page whenever it becomes obsolete. Caching

can serve up to 5000 pages/second from its **cache** on a 200 MHz PowerPC 604. This throughput is an

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memory computers without hardware support for **cache**-coherence. While existing DSM techniques are

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Source: IEEE International Symposium on High Performance Distributed Computing, Proceedings 1997. IEEE, Piscataway, NJ, USA, 97TB100183. p 264-273

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CODEN: PIDCFB **ISSN:** 1082-8907

Language: English

Document Type: CA; (Conference Article) **Treatment:** T; (Theoretical)

Journal Announcement: 9711W3

Abstract: Caching of frequently accessed data items can reduce the bandwidth requirement in a mobile wireless computing environment. Periodically broadcast of **invalidation** reports is an efficient **cache invalidation** strategy. However, this strategy is severely affected by the disconnection and mobility of the clients. In this paper, we present two adaptive **cache invalidation** report methods, in which the server broadcasts different **invalidation** reports according to the **update** and **query** rates/patterns and client disconnection time while spending little uplink cost. Simulation results show that the adaptive **invalidation** methods are efficient in improving mobile caching and reducing the uplink and downlink costs without degrading the system throughput. 16 Refs.

Descriptors: *Distributed computer systems; **Buffer** storage; Computer networks; Computer simulation; Mobile telecommunication systems; Costs

Identifiers: Adaptive **cache invalidation** methods

Classification Codes:

722.4 (Digital Computers & Systems); 722.1 (Data Storage, Equipment & Techniques); 716.3 (Radio Systems & Equipment); 911.1 (Cost Accounting); 723.5 (Computer Applications)

722 (Computer Hardware); 716 (Radar, Radio & TV Electronic Equipment); 911 (Industrial Economics); 723 (Computer Software)

72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS); 91 (ENGINEERING MANAGEMENT)

Set	Items	Description
S1	172841	CACHE? OR QUEUE? OR (TEMPORAR?) (N) (MEMOR? OR STORAGE?) OR - BUFFER?
S2	29546	INVALIDAT? OR "NOT" () (CORRECT? OR VALID?) OR EXPIRED OR IN- CORRECT?
S3	92768	REQUEST? OR QUERY OR QUERYING OR QUERIES OR QUERIED
S4	70260	UPDAT? OR UP() (DATE? OR DATING) OR REVISION? OR VERSION?
S5	814348	STATE OR STATUS OR LOG OR LOGS OR MONITOR? OR HISTORY OR H- ISTORIES
S6	118091	DATABASE? OR DATABANK? OR DATA() (BASE? OR BANK?) OR OODB? - OR DBM? OR RDB? OR DB? ?
S7	230	S1 AND S2 AND S3
S8	44	S7 AND S4
S9	17	S8 AND (S6 OR S5)
S10	44	S8 OR S9
S11	34	S10 AND IC=(G06F-012? OR G06F-017?)
S12	336	S1(4N)S2
S13	18	S11.AND S12
S14	44	S13 OR S10
S15	34	S14 AND IC=(G06F-012? OR G06F-017?)
S16	25	S15 NOT AD>20010226

File 350:Derwent WPIX 1963-2004/UD,UM &UP=200479

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16/5/7

DIALOG(R)File 350:Derwent WPIX
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013465377 **Image available**
WPI Acc No: 2000-637320/200061
XRPX Acc No: N00-472618

Cache **coherency providing method in shared memory system, involves sending acquire grant signal to requesting processor for granting exclusive use of segment to requesting processor**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: BAYLOR S J; BOLMARCICH A S; HSU Y; WU C E
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6094709	A	20000725	US 97886222	A	19970701	200061 B
TW 420772	A	20010201	TW 98103299	A	19980306	200138

Priority Applications (No Type Date): US 97886222 A 19970701

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 6094709	A	11	G06F-012/00	
TW 420772	A		G06F-011/00	

Abstract (Basic): US 6094709 A

NOVELTY - Each **cache** receiving an **invalidation request**, **invalidates** each line of a segment in the **cache**. An **invalidation** acknowledgement is then sent back to a global directory. For each line of the segment that has been modified previously, **update** data is written back to main memory. An acquire grant signal is then sent to a **requesting** processor, thus granting exclusive use of segment to the **requesting** processor.

DETAILED DESCRIPTION - Each processor in the shared memory system has an associated **cache**. The segment in each **cache** consists of more than one **cache** line. The global directory sends **invalidation** signal to all **caches** that have modified copies of all shared lines associated with the lock. The **caches** **invalidate** their copies of the line and send **invalidation** acknowledgements to the directory. Modified bit vectors associated with each **cache** line flags the modified words within a line.

USE - For providing **cache** coherency in shared memory system.

ADVANTAGE - Allows multiple critical sections involving disjoint shared variables to execute simultaneously, increasing the amount of parallelism. False sharing is reduced by enabling two distinct **caches** in a shared memory multiprocessor, lock-up free **cache** facilitates the execution of out of order memory accesses.

DESCRIPTION OF DRAWING(S) - The figure shows the coherence diagram and global **state** diagram for a line in local **cache** and global directory.

pp; 11 DwgNo 3,5/5

Title Terms: **CACHE**; COHERE; METHOD; SHARE; MEMORY; SYSTEM; SEND; ACQUIRE; SIGNAL; **REQUEST**; PROCESSOR; EXCLUDE; SEGMENT; **REQUEST**; PROCESSOR

Derwent Class: T01

International Patent Class (Main): G06F-011/00; **G06F-012/00**

File Segment: EPI

16/5/11

DIALOG(R)File 350:Derwent WPIX
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011638436 **Image available**

WPI Acc No: 1998-055344/199806

XRPX Acc No: N98-043848

Method for replacing data within computer system having skip-level cache hierarchy - updating stale copy of data in higher-level cache , thus ensuring that any copy of data remaining in that cache is consistent with updated copy of data in home location

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)

Inventor: HAGERSTEN E E; HILL M D

Number of Countries: 020 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 817079	A2	19980107	EP 97304725	A	19970630	199806 B
JP 11003280	A	19990106	JP 97184599	A	19970626	199911
US 5903907	A	19990511	US 96674560	A	19960701	199926
EP 817079	B1	20030903	EP 97304725	A	19970630	200360
DE 69724533	E	20031009	DE 624533	A	19970630	200374
			EP 97304725	A	19970630	

Priority Applications (No Type Date): US 96674560 A 19960701

Cited Patents: No-SR.Pub

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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EP 817079	A2	E	15	G06F-012/08	
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Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE

JP 11003280	A		23	G06F-012/08	
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US 5903907	A			G06F-012/08	
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EP 817079	B1	E		G06F-012/08	
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Designated States (Regional): DE FR GB IT NL SE

DE 69724533	E			G06F-012/08	Based on patent EP 817079
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Abstract (Basic): EP 817079 A

The method involves determining that a dirty copy of the data of a lower-level **cache** needs to be replaced by writing back the dirty copy from the lower-level **cache** to the home location, by **updating** the stale copy of data in the home location. The stale copy of the data in the higher-level **cache** is then **updated** or **invalidated** , thus ensuring that any copy of the data remaining in the upper-level **cache** is consistent with the **updated** copy of data in the home location.

The method further entails **requesting** an exclusive copy of the data from the home location. The dirty copy is written back from the lower-level **cache** to the home location, by **updating** the stale copy of data in the home location.

USE - In computer system memories.

ADVANTAGE - Provides flexible scheme for designating memory write back protocols for multiple level of memories within computer system for data coherency.

Dwg.1a/4

Title Terms: METHOD; REPLACE; DATA; COMPUTER; SYSTEM; SKIP; LEVEL; **CACHE** ;
HIERARCHY; **UPDATE** ; STALE; COPY; DATA; HIGH; LEVEL; **CACHE** ; ENSURE;
COPY; DATA; REMAINING; **CACHE** ; CONSISTENT; **UPDATE** ; COPY; DATA; HOME;
LOCATE

Index Terms/Additional Words: **CACHE** ONLY **MEMOR** **Y_ARC** **HITECT** **URE_N** ;

ONLY; MEMORY; ARCHITECTURE; NON-UNIFORM
Derwent Class: T01
International Patent Class (Main): **G06F-012/08**
International Patent Class (Additional): G06F-015/163
File Segment: EPI

16/5/17

DIALOG(R) File 350:Derwent WPIX
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009055921 **Image available**
WPI Acc No: 1992-183311/199222
XRPX Acc No: N92-138370

**Multiple-level multiprocessor cache memory organisation method -
defining status of each cache with tag bit and updating tag bits
with instruction execution**

Patent Assignee: PRIME COMPUTER INC (PRIM)
Inventor: ALBONESI D H; CHANG J; FAASE J G; HOMBERG M J; LANGENDORF B K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5113514	A	19920512	US 89397124	A	19890822	199222 B
			US 90482288	A	19900220	

Priority Applications (No Type Date): US 90482288 A 19900220; US 89397124 A 19890822

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5113514	A	43	G06F-012/00	Cont of application US 89397124

Abstract (Basic): US 5113514 A

The method of maintaining coherence amongst a number of devices involves attaching tag bits to each data block stored in a **cache** to indicate the condition of the block w.r.t. other copies of the block in the multi-processor system. The conditions that may arise are (1) invalid, (2) shared, (3) private, and (4) modified. The invalid **status** indicates that the data copy may be **incorrect** while the shared **status** indicates that the data copy is correct and equivalent to the main memory copy and other **caches** may also contain a correct copy. The private **status** indicates that the data copy is correct and equivalent to main memory copy, but it not contained in any other **cache**, while the modified **status** indicates that the copy is not equivalent to the memory data block, and no other **cache** has a valid copy.

When a processor operates on a data block, its associated **cache** sends an instruction via the system bus to all system devices to identify the block and the operation. Each system device **cache** will respond to the instruction to indicate if it holds a data copy. The **cache** responses are assimilated into a collective response message to define the condition of the data block and the tag bits of the original instruction and **updated** accordingly. The other **cache** tag bits are modified in line with the execution of the instruction. A READ instruction **requesting** a valid copy of a data block for a **cache** may change the tag bits attached to a block depending on its original **status**.

ADVANTAGE - Use of system bus for accessing memory locations is minimised. **Cache** consistency maintained while providing efficient addressing protocol. Decentralised **cache** system avoids catastrophic failure in event of fault at single point.

Dwg.1/16

Title Terms: MULTIPLE; LEVEL; MULTIPROCESSOR; **CACHE**; MEMORY; ORGANISE; METHOD; DEFINE; **STATUS**; **CACHE**; TAG; BIT; **UPDATE**; TAG; BIT; INSTRUCTION; EXECUTE

Derwent Class: T01

International Patent Class (Main): G06F-012/00

International Patent Class (Additional): G06F-013/00

File Segment: EPI

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16/5/20

DIALOG(R) File 350:Derwent WPIX.
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008541477 **Image available**
WPI Acc No: 1991-045540/199107
XRPX Acc No: N91-035502

**Multiprocessor cache system - uses three states, invalid, and updated
, to control invalidating signals**

Patent Assignee: HITACHI LTD (HITA)

Inventor: AOKI H; HATANNO S; KITANO J; NISHII O; OISHI K; UCHIYAMA K; KITANO

Number of Countries: 005 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 412353	A	19910213	EP 90114195	A	19900724	199107 B
EP 412353	A3	19920527	EP 90114195	A	19900724	199331
US 5283886	A	19940201	US 90556119	A	19900720	199406
			US 92950746	A	19920924	

Priority Applications (No Type Date): JP 89206773 A 19890811

Cited Patents: NoSR.Pub; 2.Jnl.Ref; EP 301354; FR 2430637

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 412353	A				

Designated States (Regional): DE FR GB IT

US 5283886 A 28 G06F-012/12 Cont of application US 90556119

Abstract (Basic): EP 412353 A

The multiprocessor system has two **caches** controlled by two processors and an address bus, a data bus, an **invalidating** signal line and a main memory. There are three states for data in the **caches**, the first is 'invalid', the second is 'valid but not **updated**' and the third is 'valid and **updated**'. When write access from a processor hits a **cache** the **state** is shifted from second to third and the **cache** outputs the address of the write hit to the address bus and an **invalidating** signal to the **invalidating** signal line.

When an access misses a **cache** a block of data is transferred from main memory to the **cache**, and the **invalidating** signal is put out.

ADVANTAGE - Avoids many of the problems of conventional multiprocessor **cache** systems. (34pp Dwg.No.1/10)

Title Terms: MULTIPROCESSOR; **CACHE** ; SYSTEM; THREE; **STATE** ; INVALID;
UPDATE ; CONTROL; INVALID; SIGNAL

Derwent Class: T01

International Patent Class (Main): G06F-012/12

International Patent Class (Additional): G06F-012/08

File Segment: EPI

18/5/15 (Item 2 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online
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01710663 ORDER NO: AADAA-I9946009

Improving cache performance with adaptive cache topologies and deferred coherence models

Author: Lee, Yongjoon

Degree: Ph.D.

Year: 1999

Corporate Source/Institution: University of Florida (0070)

Chair: Jih-Kwon Peir

Source: VOLUME 60/09-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 4709. 155 PAGES

Descriptors: COMPUTER SCIENCE

Descriptor Codes: 0984

Memory references exhibit locality and are therefore not uniformly distributed across the sets of a **cache**. This skew reduces the effectiveness of a **cache** because it results in the caching of a considerable number of less-recently used lines. In this dissertation, a technique that dynamically identifies these less-recently used lines and effectively utilizes the **cache** frames is described. These underutilized **cache** frames can be occupied by the more-recently used **cache** lines. Also, these frames can be used to further reduce the miss ratio through data prefetching. In the proposed design, the possible locations that a line can reside in is not predetermined. Instead, the **cache** is dynamically partitioned into groups. Because both the number of groups and each group associativity adapt to the dynamic reference pattern, this design is called the adaptive group-associative **cache**. This new adaptive **cache** topology utilizes the **cache** frames. Performance evaluation shows the group-associative **cache** is able to achieve a hit ratio better than that of a 4-way set-associative **cache**. For some of the SPEC95 workloads, the hit ratio approaches that of a fully associative **cache**.

Private **caches** are a critical component to hide memory access latency in high performance multiprocessor systems. However, multiple processors may concurrently **update** a distinct portion of a **cache** line and cause unnecessary **cache invalidations** under traditional **cache** coherence protocols.

In this dissertation research, a deferred **cache** coherence model is proposed, which allows a **cache** line to be shared in multiple **caches** in the inconsistent **state** as long as the processors are guaranteed not to access any stale data. Multiple write **requests** to different portions of a **cache** line can be performed locally without **invalidation**. An efficient mechanism to reconcile multiple inconsistent copies of the modified line is described to satisfy the data dependence. This new **cache** coherence model minimizes the **cache** coherence activities. Simulation results show that the proposed **cache** coherence model improves the performance of the parallel applications compared to conventional MESI and delayed coherence protocol up to 30%.

18/5/16 (Item 3 from file: 35)

DIALOG(R)File 35:Dissertation Abs Online
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01520041 ORDER NO: AAD96-38182

DATA CONSISTENCY MANAGEMENT IN WIRELESS CLIENT-SERVER INFORMATION SYSTEMS

Author: JING, JIN

Degree: PH.D.

Year: 1996

Corporate Source/Institution: PURDUE UNIVERSITY (0183)

Major Professor: AHMED K. ELMAGARMID

Source: VOLUME 57/07-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 4514. 146 PAGES

Descriptors: COMPUTER SCIENCE ; ENGINEERING, ELECTRONICS AND ELECTRICAL

Descriptor Codes: 0984; 0544

The emerging mobile computing environment no longer requires a user to maintain a fixed position in the network and thus allows for almost unrestricted user mobility. In the near future, users carrying portable devices will have access to information systems independent of the users' physical locations. This thesis proposes and investigates new techniques to provide high performance and scalability for these information systems while maintaining data consistency semantics in wireless and mobile computing environments. The common theme of the techniques developed is the utilization of mobile and fixed host resources through data replication (or cache) and partition.

The initial chapters motivate and describe an indirect interaction architecture for wireless client-server information systems and present the arguments for using data replication, partition, and cache as the basis for constructing the wireless client-server information systems. The rest of the thesis then focuses on the development and performance analysis of algorithms for replicated and partitioned data management in fixed data servers and cached data management in mobile clients.

A new algorithm that uses a "deferred **log update**" technique is developed for the replicated data management. A performance analysis shows that the algorithm can provide improved performance over traditional replicated data management algorithms in mobile environments. The "deferred **log update**" technique is further applied in the development of a partitioned data management algorithm. The algorithm is compared with other conventional protocols under different workload conditions. The reliability issues in applying the technique are examined.

For cached data management, a broadcast based **cache invalidation** algorithm is resented. The algorithm uses "**update** aggregation" and "bit-sequence naming" techniques to reduce the broadcast message size. This algorithm trades the precision of invalidation for the speed of invalidation. Two extensions of the algorithm are designed for large **databases**. A simulation study of the proposed algorithm and its extensions is then presented. The study shows that the proposed algorithm can perform consistently well under conditions of variable **update** rates/patterns and client disconnection times and the two extensions can scale well to large **databases** for the "information feed" application domain with skewed access pattern.

18/5/34 (Item 16 from file: 2)

DIALOG(R)File 2:INSPEC

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4643579 INSPEC Abstract Number: C9405-5440-018

Title: An enhanced write- invalidate snooping cache coherence protocol for multiprocessor systems with split transaction bus

Author(s): Jhang Seong Tae; Jhon Chu Shik

Journal: Journal of the Korea Information Science Society vol.21, no.1
p.53-65

Publication Date: Jan. 1994 Country of Publication: South Korea

CODEN: HJKHDC ISSN: 0258-9125

Language: Korean Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: We present a new write- **invalidate** snooping **cache** coherence protocol called MMESSII (modified, modified-shared, exclusive, shared-source, shared, invalid-by-other, invalid) cache protocol which addresses several significant drawbacks of existing write- **invalidate** snooping **cache** coherence protocols under the split transaction bus based multiprocessor environment. In this protocol, each cache block maintains the ID information to identify the processor module that invalidated the block most recently. It also maintains one of seven cache states which consist of two **updated** states (MODIFIED, MODIFIED-SHARED), one exclusive **state** (EXCLUSIVE), two shared states (SHARED-SOURCE, SHARED) and two invalidated states (INVALID-BY-OTHER, INVALID). By using these states and the ID information, the protocol reduces the contention for both memory modules and system bus significantly, and also provides the fast cache-to-cache response. (27 Refs)

Subfile: C

Descriptors: buffer storage; multiprocessing systems; protocols; system buses

Identifiers: enhanced write- **invalidate** snooping **cache** coherence protocol; multiprocessor systems; split transaction bus; write- **invalidate** snooping **cache** coherence protocol; MMESSII; multiprocessor environment; cache block; ID information; cache states; **updated** states; exclusive **state** ; shared states; invalidated states; memory modules; system bus; fast cache-to-cache response

Class Codes: C5440 (Multiprocessor systems and techniques); C5610S (System buses); C5220P (Parallel architecture); C5320G (Semiconductor storage)

Set	Items	Description
S1	424777	CACHE? OR QUEUE? OR (TEMPORAR?) (N) (MEMOR? OR STORAGE?) OR - BUFFER?
S2	84829	INVALIDAT? OR "NOT" () (CORRECT? OR VALID?) OR EXPIRED OR IN- CORRECT?
S3	246036	REQUEST? OR QUERY OR QUERYING OR QUERIES OR QUERIED
S4	805820	UPDAT? OR UP () (DATE? OR DATING) OR REVISION? OR VERSION?
S5	6710086	STATE OR STATUS OR LOG OR LOGS OR MONITOR? OR HISTORY OR H- ISTORIES
S6	1047934	DATABASE? OR DATABANK? OR DATA () (BASE? OR BANK?) OR OODB? - OR DBM? OR RDB? OR DB? ?
S7	240	S1 AND S2 AND S3
S8	100	S7 AND S4
S9	45	S8 AND (S6 OR S5)
S10	100	S8 OR S9
S11	177	S1(2N)S2 AND S4
S12	54	S11 AND S6
S13	27	S11 AND S5
S14	46	S11 AND S10
S15	92	S12 OR S13 OR S14
S16	60	RD (unique items)
S17	40	S16 NOT PY>2001
S18	39	S17 NOT PD>20010226
File	8: Ei Compendex(R)	1970-2004/Nov W4 (c) 2004 Elsevier Eng. Info. Inc.
File	35: Dissertation Abs Online	1861-2004/Nov (c) 2004 ProQuest Info&Learning
File	202: Info. Sci. & Tech. Abs.	1966-2004/Nov 02 (c) 2004 EBSCO Publishing
File	65: Inside Conferences	1993-2004/Dec W2 (c) 2004 BLDSC all rts. reserv.
File	2: INSPEC	1969-2004/Dec W1 (c) 2004 Institution of Electrical Engineers
File	94: JICST-EPlus	1985-2004/Nov W1 (c) 2004 Japan Science and Tech Corp(JST)
File	111: TGG Natl. Newspaper Index(SM)	1979-2004/Dec 09 (c) 2004 The Gale Group
File	233: Internet & Personal Comp. Abs.	1981-2003/Sep (c) 2003 EBSCO Pub.
File	6: NTIS	1964-2004/Dec W1 (c) 2004 NTIS, Intl Cpyrght All Rights Res
File	144: Pascal	1973-2004/Dec W1 (c) 2004 INIST/CNRS
File	434: SciSearch(R) Cited Ref Sci	1974-1989/Dec (c) 1998 Inst for Sci Info
File	34: SciSearch(R) Cited Ref Sci	1990-2004/Dec W1 (c) 2004 Inst for Sci Info
File	99: Wilson Appl. Sci & Tech Abs	1983-2004/Nov (c) 2004 The HW Wilson Co.
File	95: TEME-Technology & Management	1989-2004/Jun W1 (c) 2004 FIZ TECHNIK

18/5/1 (Item 1 from file: 8)

DIALOG(R) File 8: Ei Compendex(R)

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05855655 E.I. No: EIP01306590842

Title: Mobile client caching with asynchronous broadcasting

Author: Chung, I.Y.; Hwang, C.-S.; Jung, S.Y.

Corporate Source: Dept. of Comp. Sci. and Eng. Korea University, Seongbuk-gu, Seoul 136-701, South Korea

Source: International Journal of Parallel and Distributed Systems and Networks v 4 n 2 2001. p 85-93 204-0157

Publication Year: 2001

CODEN: IJPNFY **ISSN:** 1206-2138

Language: English

Document Type: JA; (Journal Article) **Treatment:** G; (General Review)

Journal Announcement: 0107W4

Abstract: In mobile client-server **database** systems, caching of frequently accessed data is an important technique that will reduce contention on the narrow bandwidth wireless channel. As the server in mobile environments may not have any information about the **state** of its clients' cache (stateless server), using broadcasting approach to transmit the **updated** data lists to numerous concurrent mobile clients is an attractive approach. In this article, a caching policy is proposed to maintain cache consistency for mobile computers. The proposed protocol adopts asynchronous (nonperiodic) broadcasting as the **cache invalidation** scheme, and supports transaction semantics in mobile environments. With the asynchronous broadcasting approach, the proposed protocol can improve the throughput by reducing the abortion of transactions with low communication costs. We study the performance of the protocol by means of simulation experiments. 15 Refs.

Descriptors: *Network protocols; **Database** systems; Client server computer systems; Mobile computing; Cache memory; Concurrency control; Congestion control (communication); Telecommunication traffic; Data communication systems

Identifiers: Mobile client caching; Asynchronous broadcasting; Mobile **databases** ; Transaction processing

Classification Codes:

723.5 (Computer Applications); 723.3 (Database Systems); 722.4 (Digital Computers & Systems); 722.1 (Data Storage, Equipment & Techniques); 716.1 (Information & Communication Theory)

723 (Computer Software, Data Handling & Applications); 722 (Computer Hardware); 716 (Electronic Equipment, Radar, Radio & Television)

72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATION ENGINEERING)

18/5/2 (Item 2 from file: 8)

DIALOG(R) File 8: Ei Compendex(R).

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05165578 E.I. No: EIP98114482503

Title: **Energy-efficient mobile** cache invalidation

Author: Wu, Kun-Lung; Yu, Philip S.; Chen, Ming-Syan

Corporate Source: IBM T.J. Watson Research Cent, Yorktown Heights, NY, USA

Source: Distributed and Parallel Databases v 6 n 4 Oct 1998. p 351-372

Publication Year: 1998

CODEN: DAATES ISSN: 0926-8782

Language: English

Document Type: JA; (Journal Article) Treatment: T; (Theoretical)

Journal Announcement: 9901W3

Abstract: Caching data in a wireless mobile computer can significantly reduce the bandwidth requirement. However, due to battery power limitation, a wireless mobile computer may often be forced to operate in a doze or even totally disconnected mode. As a result, the mobile computer may miss some **cache invalidation** reports. In this paper, we present an energy-efficient **cache invalidation** method for a wireless mobile computer. The new **cache invalidation** scheme is called grouping with cold **update** -set retention (GCORE). Upon waking up, a mobile computer checks its **cache** validity with the server. To reduce the bandwidth requirement for validity checking, data objects are partitioned into groups. However, instead of simply **invalidating** a group if any of the objects in the group has been **updated**, GCORE retains the cold **update** set of objects in a group if possible. We present an efficient implementation of GCORE and conduct simulations to evaluate its caching effectiveness. The results show that GCORE can substantially improve mobile caching by reducing the communication bandwidth (thus energy consumption) for **query** processing. (Author abstract) 11 Refs.

Descriptors: *Mobile computing; **Buffer** storage; Electric power supplies to apparatus; Client server computer systems; Computer simulation; Bandwidth

Identifiers: Wireless mobile computer; **Cache invalidation** method; Grouping with cold **update** set retention

Classification Codes:

723.5 (Computer Applications); 722.1 (Data Storage, Equipment & Techniques); 713.5 (Other Electronic Circuits); 722.4 (Digital Computers & Systems)

723 (Computer Software); 722 (Computer Hardware); 713 (Electronic Circuits)

72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

18/5/7 (Item 7 from file: 8)
DIALOG(R)File 8: Ei Compendex(R).
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04720843 E.I. No: EIP97063692568

Title: Effectiveness of hardware-based and compiler-controlled snooping cache protocol extensions

Author: Dahlgren, Fredrik; Skeppstedt, Jonas; Stenstrom, Per

Corporate Source: Lund Univ, Lund, Sweden

Source: Doktorsavhandlingar vid Chalmers Tekniska Hogskola n 1280 1997.

6pp

Publication Year: 1997

CODEN: DCTHAT ISSN: 0346-718X

Language: English

Document Type: RR; (Report Review) Treatment: T; (Theoretical)

Journal Announcement: 9708W1

Abstract: Cache misses and memory traffic limit the performance of bus-based multiprocessors using invalidation-based snooping caches. This motivates us to consider hardware-based and compiler-controlled cache protocol extensions that cut the number of misses and/or bus traffic. Controlled updating of remote cache copies is the approach used to attack coherence misses and encompasses a hybrid update / invalidate protocol and a compiler-controlled update scheme. Coalescing of ownership acquisition with miss handling is the approach to eliminate invalidation traffic. A simple hardware heuristic known as migrate-on-dirty, an adaptive hardware-based scheme, and compiler-controlled insertion of load-exclusive requests use this approach. We evaluate the relative effectiveness of these schemes using detailed architectural simulations and a set of four parallel programs. Whereas both schemes using controlled updating are equally effective in removing coherence misses, the hybrid update / invalidate scheme does this at a lower traffic level. As for the invalidation traffic reduction, however, the compiler-based scheme is slightly more efficient than the adaptive hardware-based scheme. By contrast, migrate-on-dirty is shown to have devastating effects on the miss rate for some applications. (Author abstract) 13 Refs.

Descriptors: *Network protocols; Buffer storage; Program compilers; Multiprocessing systems; Telecommunication traffic; Computer hardware; Computer simulation

Identifiers: Snooping caches; Cache misses; Coherence misses; Ownership acquisition; Parallel programs

Classification Codes:

723.2 (Data Processing); 722.1 (Data Storage, Equipment & Techniques); 723.1 (Computer Programming); 722.4 (Digital Computers & Systems); 716.1 (Information & Communication Theory); 723.5 (Computer Applications)
723 (Computer Software); 722 (Computer Hardware); 716 (Radar, Radio &

TV Electronic Equipment)

72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

18/5/11 (Item 11 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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03850394 E.I. No: EIP94051276760

Title: New write- invalidate snooping cache coherence protocol for split transaction bus-based multiprocessor systems

Author: Jhang, Seong Tae; Jhon, Chu Shik

Corporate Source: Seoul Natl Univ, Seoul, S Korea

Conference Title: Proceedings of the 1993 IEEE Region 10 Conference on Computer, Communication, Control and Power Engineering (TENCON '93). Part 1 (of 5)

Conference Location: Beijing, China Conference Date: 19931019-19931021

Sponsor: IEEE

E.I. Conference No.: 20220

Source: Proceedings of the 10th IEEE Region Conference on Computer, Communication, Control and Power Engineering Proc 1993 IEEE Reg 10 Conf Comput Commun Control Power Eng (TENCON '93) 1993. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. p 229-232

Publication Year: 1993

ISBN: 0-7803-1233-3

Language: English

Document Type: CA; (Conference Article) Treatment: G; (General Review); T; (Theoretical)

Journal Announcement: 9406W2

Abstract: In this paper, we present a new write- **invalidate** snooping **cache** coherence protocol called MMESSII cache protocol which addresses several significant drawbacks of existing write-invalidate snooping protocols under the split transaction bus based multiprocessor environment. In this protocol, each cache block maintains the ID information to identify the processor module that invalidated the block most recently. It also maintains seven cache states which consist of two **updated** states, one exclusive **state**, two shared states and two invalidated states. By using these states and the ID information, our protocol can reduce the contention for both memory modules and system bus significantly. We also present the simulation results which show better performance of our protocol than that of existing write-invalidate protocols. (Author abstract) 16 Refs.

Descriptors: *Network protocols; Computer networks; Multiprocessing systems; Data storage equipment; Storage allocation (computer); **State** assignment; Performance; Program processors

Identifiers: Write **invalidate** snooping **cache** coherence protocol; Split transaction bus based multiprocessor systems; MMESSII cache protocol; Shared memory multiprocessor systems

Classification Codes:

723.1 (Computer Programming); 723.2 (Data Processing); 722.4 (Digital Computers & Systems); 722.3 (Data Communication, Equipment & Techniques); 722.1 (Data Storage, Equipment & Techniques); 721.1 (Computer Theory, Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory)

723 (Computer Software); 722 (Computer Hardware); 721 (Computer Circuits & Logic Elements)

72 (COMPUTERS & DATA PROCESSING)

18/5/12 (Item 12 from file: 8)
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02940925 E.I. Monthly No: EI9008090490

Title: **Asynchronous multicaches.**

Author: Brown, Geoffrey M.

Corporate Source: Cornell Univ, Ithaca, NY, USA

Source: Distributed Computing v 4 n 1 Mar 1990 p 31-36

Publication Year: 1990

CODEN: DICOEB ISSN: 0178-2770

Language: English

Document Type: JA; (Journal Article) Treatment: T; (Theoretical)

Journal Announcement: 9008

Abstract: In previous multicache consistency mechanisms, processors have been required to synchronize with all **caches** when **updating** shared data. This synchronization occurs while **invalidating** inconsistent copies of the data. We present a simple **cache** consistency mechanism which demonstrates that this synchronization is unnecessary. In particular, we show that it is possible to **buffer invalidation requests** at the **caches** while guaranteeing that concurrent programs are correctly executed by the system. This offers increased processor utilization by allowing the **caches** to handle **invalidation requests** between accesses by their associated processors. In addition, **buffering invalidation requests** offers greater utilization of shared memory by speeding up store operations. Additional contributions of this paper are the development of a formal definition of consistency and of a technique for proving that a system is consistent. (Author abstract) 10 Refs.

Descriptors: ***DATABAS E SYSTEMS--*Distributed; COMPUTER SYSTEMS, DIGITAL --Distributed**

Identifiers: ASYNCHRONOUS MULTICACHES; MULTICACHE CONSISTENCY MECHANISMS;
CACHE CONSISTENCY

Classification Codes:

723 (Computer Software)

72 (COMPUTERS & DATA PROCESSING)

Set	Items	Description
S1	290951	CACHE? OR QUEUE? OR (TEMPORAR?) (N) (MEMOR? OR STORAGE?) OR - BUFFER?
S2	38710	INVALIDAT? OR "NOT"() (CORRECT? OR VALID?) OR EXPIRED OR IN- CORRECT?
S3	193543	REQUEST? OR QUERY OR QUERYING OR QUERIES OR QUERIED
S4	117094	UPDAT? OR UP() (DATE? OR DATING) OR REVISION? OR VERSION?
S5	2186105	STATE OR STATUS OR LOG OR LOGS OR MONITOR? OR HISTORY OR H- ISTORIES
S6	175783	DATABASE? OR DATABANK? OR DATA() (BASE? OR BANK?) OR OODB? - OR DBM? OR RDB? OR DB? ?
S7	452	S1 AND S2 AND S3
S8	69	S7 AND S4
S9	30	S8 AND (S6 OR S5)
S10	69	S8 OR S9
S11	53	S10 AND IC=(G06F-012? OR G06F-017?)
S12	652	S1(4N)S2
S13	27	S11 AND S12

File 347:JAPIO Nov 1976-2004/Aug(Updated 041203)

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File 350:Derwent WPIX 1963-2004/UD,UM &UP=200479

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13/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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06397096 **Image available**
INPUT/OUTPUT BUFFER SYSTEM AND INPUT/OUTPUT BUFFER CONTROL METHOD
BETWEEN PLURAL HOST COMPUTERS

PUB. NO.: 11-338747 [JP 11338747 A]
PUBLISHED: December 10, 1999 (19991210)
INVENTOR(s): UKO JUNYA
ONO SATOSHI
APPLICANT(s): NEC SOFTWARE LTD
NEC CORP
APPL. NO.: 10-139532 [JP 98139532]
FILED: May 21, 1998 (19980521)
INTL CLASS: G06F-012/00 ; G06F-013/00

ABSTRACT

PROBLEM TO BE SOLVED: To delete input operation from an external storage device by **buffering** by providing a common file control means for the other host computer when the host computers share a file and maintaining the consistency to data on the common file.

SOLUTION: The host computers 1 and 2 are connected by a fast communication bus 70 and shares a magnetic disk drive 8. When the host computer 1 **updates** data 82 in the common file 81 on the magnetic disk drive 8 in this **state**, the host computer 1 turns off a **buffer** presence flag 66 of a **buffer** control table 65 regarding a **buffer** area 67 for data 82 of the host computer 2 and sends a **request** to **invalidates** the **buffer** area 67 to the host computer 2 before performing a writing process to the common file 81. The host computer 1 after being informed of success by the host computer 2 and confirming that writes the data to the magnetic disk drive 8.

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13/5/5 (Item 5 from file: 347)
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04043891 **Image available**
CACHE MEMORY DEVICE

PUB. NO.: 05-035591 [JP 5035591 A]
PUBLISHED: February 12, 1993 (19930212)
INVENTOR(s): GOSHIMA TATSUHIRO
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 03-188815 [JP 91188815]
FILED: July 29, 1991 (19910729)
INTL CLASS: [5] G06F-012/08 ; G06F-012/08
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 1560, Vol. 17, No. 326, Pg. 44, June
21, 1993 (19930621)

ABSTRACT

PURPOSE: To maximally utilize the high-speed access performance that a small-capacity virtual cache has, the high hit rate that a large-capacity physical cache has and the easiness of cache entry invalidation .

CONSTITUTION: A virtual cache 2 and a TLB 4 are accessed at a load request from an arithmetic control part and when the cache 2 is mishit, a physical cache 7 is accessed with a physical address obtained through the conversion of the TLB 4. Data of its entry are outputted selectively to the arithmetic control part and registered in a mishit entry in the virtual cache 2 under the control of a control part 10. When a main storage is updated by another processor, the physical cache 7 is accessed with its write address and when the cache is hit, the hit entry and all entries of the small-capacity virtual cache 2 corresponding to the entry are invalidated .

13/5/6 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO
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03826846 **Image available**
SNOOP CACHE MEMORY CONTROL SYSTEM

PUB. NO.: 04-191946 [JP 4191946 A]
PUBLISHED: July 10, 1992 (19920710)
INVENTOR(s): SATO MASAKI
YAMAMOTO AKIRA
OHARA TERUHIKO
TAKEDA KOICHI
APPLICANT(s): AGENCY OF IND SCIENCE & TECHNOL [000114] (A Japanese
Government or Municipal Agency), JP (Japan)
APPL. NO.: 02-320914 [JP 90320914]
FILED: November 27, 1990 (19901127)
INTL CLASS: [5] G06F-012/08
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 1444, Vol. 16, No. 520, Pg. 49,
October 26, 1992 (19921026)

ABSTRACT

PURPOSE: To improve the utilizing efficiency of a common bus by dynamically discriminating whether a **cache** memory having a same block is to be revised or **invalidated** based on an operating **state** of the block of a processor when a common data in other **cache** memory is rewritten.

CONSTITUTION: A flag (access flag) 20 set when a processor accesses a block in a **cache** memory 13 once or over is provided in the unit of blocks. When its own access flag is set up to a point of time when a same block of other **cache** memory is rewritten, its own block is revised but when the access flag 20 is not set, its own block is **invalidated** and the consistency is maintained by giving information representing whether the block is revised or **invalidated** to the **cache** memory 13 being a **revision request** source. Thus, undesired **revision** of the common block is minimized in this way to improve the utilizing efficiency of the common bus 80.